1.4 GBd Transmitter/Receiver Chip Set with CIMT Encoder/Decoder and Variable Data Rate

Technical Data

September 7, 1999 (Rev 1.26)

HDMP-1032 Transmitter
HDMP-1034 Receiver

Features

· **3.3 V Supply, Low Power Dissipation**
590 mW Tx, 660 mW Rx

· **On-Chip Encode / Decode using Conditional Inversion Master Transition (CIMT) Protocol**

· **1:N Broadcast Ready**
Configurable Receiver Inputs allow Multi-Point Data Broadcast using a Single Transmitter

· **Parallel Automatic Synchronization System (PASS)**
Allows Receiver to Read Recovered Words with Local Reference Clock

· **Robust Simplex Mode**

· **Wide Range Serial Rate**
260-1400 MBaud (User Selectable)

· **5 V Tolerant TTL Interface**
16 or 17 Bits Wide

· **Low Cost 64 Pin Plastic Package**
14x14 mm^2 PQFP

Applications

· **Cellular Base Station**
· **ATM Switch**
· **Backplane/Bus Extender**
· **Video, Image Acquisition**
· **Point to Point Data Link**
· **Implement SCI-FI Standard**

Description

The HDMP-1032 transmitter and HDMP-1034 receiver are used together to build a high-speed data link for point-to-point communication. These silicon bipolar transmitter and receiver chips are housed in standard plastic 64 pin PQFP packages.

From the user's viewpoint, these products can be thought of as a "virtual ribbon cable" interface for the transmission of data and control words. A parallel word loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel and is then reconstructed into its original parallel form. The channel can be either a coaxial copper cable or optical link

The chip set hides from the user the complexity of encoding, multiplexing, clock extraction, demultiplexing and decoding. The CIMT encoding scheme used ensures the DC balance of the serial line. When data or control words are not being sent the transmitter sends idle words.

The serial data rate of the Tx/Rx link is selectable in three ranges and extends from 208 to 1120 Mbit/s. This translates into an encoded serial rate of 260 to 1400 MBaud. The parallel data interface is 16 bit TTL. A flag bit is also present and can be used as an extra 17^{th} bit under the user's control. This bit can be used as an even or odd word indicator for dual-word

transmission. The encoding of the flag bit can be

CAUTION: As with all semiconductor ICs, it is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).

scrambled to reduce the probability of erroneous word alignment.

A user control space is also provided. If TXCNTL is asserted on the Tx chip, the least significant 14 bits of the data will be sent and the RXCNTL line on the Rx chip will indicate the data is a Control Word.

At the Rx, the PASS feature allows the recovered words to be clocked out with the local REFCLK. This feature is particularly useful when the Tx clock and REFCLK are synchronous. The PASS system also supports synchronization of multiple channels.

The chipset is compatible with previous versions of the G-Link chipset (HDMP-10x2/10x4) provided the latter are used in 16 bit Simplex with Periodic Sync Pulse or External Reference Oscillator Mode (Simplex Method II or III).

Table of Contents

Typical Applications

The HDMP-1032/1034 chipset was designed for ease of use and flexibility. The customer can tailor the use of this product through the configuration of the link based on specific system requirements and application needs. Typical applications range from backplane serialization and bus extension to cellular base stations.

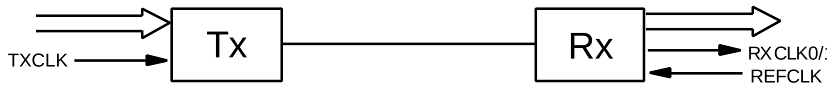
All modes are built up from the basic simplex transmission mode as shown in Figure 1a.

For digital video transmission, simplex links are common. The HDMP-1032/1034 chipset can transmit 16 bits of parallel data in standard or broadcast simplex mode (Figures 1a, 1b).

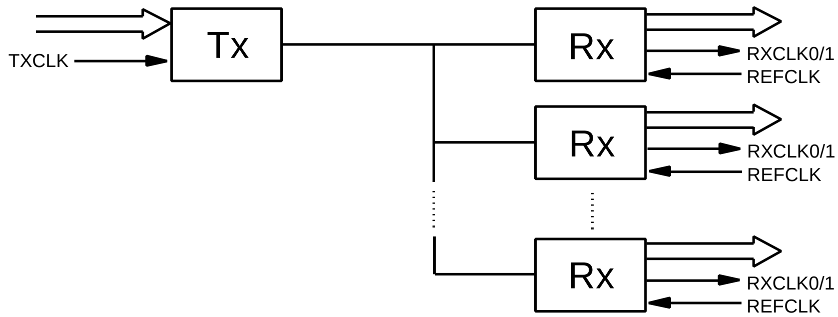
If the bus is 32 bits wide, the HDMP-1032/1034 chipset is capable of sending this data word as two separate word segments with the use of an external mux and demux as shown in Figure 1c. In this mode, the transmitter and receiver use the FLAG bit to indicate the first or second word segment. The HDMP-1032/1034 chipset may also be configured in full duplex to achieve a 32 bit wide bus extension. In addition, 32 bit wide data can be transmitted over two parallel serial lines as shown in Figure 1d.

Low latency bus extension of a 16 bit wide data bus may be achieved using the full duplex configuration (Figure 1e). In this mode, link startup is achieved by exchange of control words.

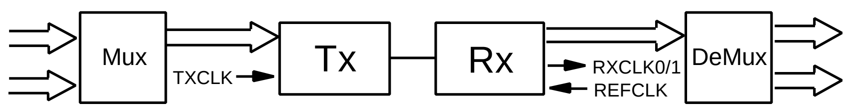
The HDMP-1032/1034 chipset can support serial transmission rates from 260 MBd to 1.40 GBd for each of these configurations. The chipset requires the user to input the link data rate by asserting accordingly the DIV1/0 pins on both the Tx and Rx. To determine the DIV1/0 settings necessary for each application, refer to the section *Setting the Operating Data Rate Range* on the next page.



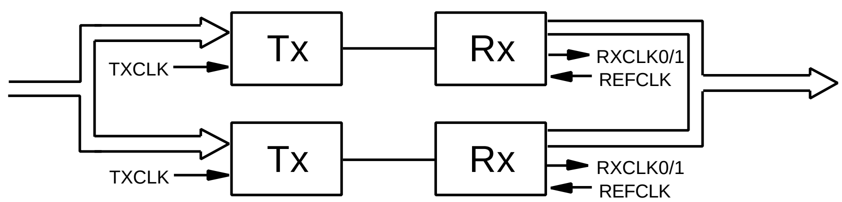
a) 16 Bit Simplex Transmission



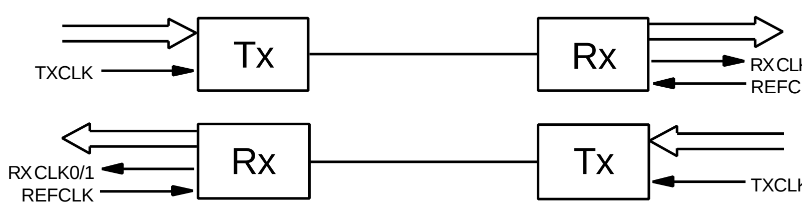
b) 16 Bit Broadcast Transmission



c) 32 Bit Simplex Transmission



d) 32 Bit Simplex Transmission



e) 16 Bit Duplex Transmission

Figure 1. Various Configurations using the HDMP-1032/1034

Setting the Operating Data Rate Range

The HDMP-1032/1034 chipset can operate from 260 MBaud to 1400 MBaud. It is divided into three operating data ranges with each range selected by setting DIV1/0 as shown in the *Typical Operating Rates* table below. Two examples have been provided in order to help in understanding and using this table.

Example 1 (Unique Range)

It is desired to transmit a 16 bit parallel word operating at a frequency of 60 MHz (60 MWord/sec). Both the Tx and Rx must be set to a range that covers this word rate. According to the table only a setting of DIV1/0 = (0/0) allows a parallel input word rate of 40 to 70 MHz. This range setting easily accommodates the required 60 MHz word rate and is unique. The user serial data rate is calculated as:

$$\mathit{Serial\ Data\ Rate} = \left(\frac{16\mathit{bits}}{\mathit{Word}}\right)\left(\frac{60\mathit{MW}}{\mathrm{sec}}\right) = 960\ \mathit{MBits}/\mathrm{sec}$$

The baud rate includes an additional four encoding bits (20 bits total) that the HDMP-1032/34 G-Link chipset transmits. The serial baud rate is calculated as:

$$\mathit{Serial\ Baud\ Rate} = \left(\frac{20\mathit{bits}}{\mathit{Word}}\right)\left(\frac{60\mathit{MW}}{\mathrm{sec}}\right) = 1200\ \mathit{MBaud}$$

Example 2 (Overlapping Ranges)

Some applications may have a parallel word rate that seems to fit in two ranges of operation. For example, a 42.5 MHz (42.5 MWord/s) parallel data rate falls within two ranges: DIV1/0 = (0/0) and DIV1/0 = (0/1). According to the table, a setting of DIV1/0 = (0/1) gives an upper rate of 45 MHz while a setting of DIV1/0 = (0/0) gives a lower rate of 40 MHz. The upper and lower data rates stated in the tables are typical values unless indicated by (min) or (max) and may vary between individual parts. However, each transmitter/receiver has overlapping ranges of operation providing continuous band coverage from 260 to 1400 MBaud.

In this example, each transmitter/receiver will permit a 42.5 MHz parallel data rate but it is suggested that DIV0 be tied to a jumper that can be set either to logic '1' (open allowing DIV0 to float high) or logic '0' (ground). This allows the design to accommodate both ranges for maximum flexibility. This technique is recommended whenever operating near the upper and lower ends of two adjacent word rate ranges.

HDMP-1032 (Tx), HDMP-1034 (Rx) Typical Operating Rates[1,2]

Tc = 0 °C to +85 °C, V_{CC} = 3.15V to 3.45V

DIV1	DIV0	Parallel Word Rate (MWord/sec)		Serial Data Rate (MBits/sec)		Serial Baud Rate (MBaud)	
		Range		Range		Range	
0	0	40	70 (max)	640	1120 (max)	800	1400 (max)
0	1	20	45	320	720	400	900
1	0	13 (min)	26	208 (min)	416	260 (min)	520

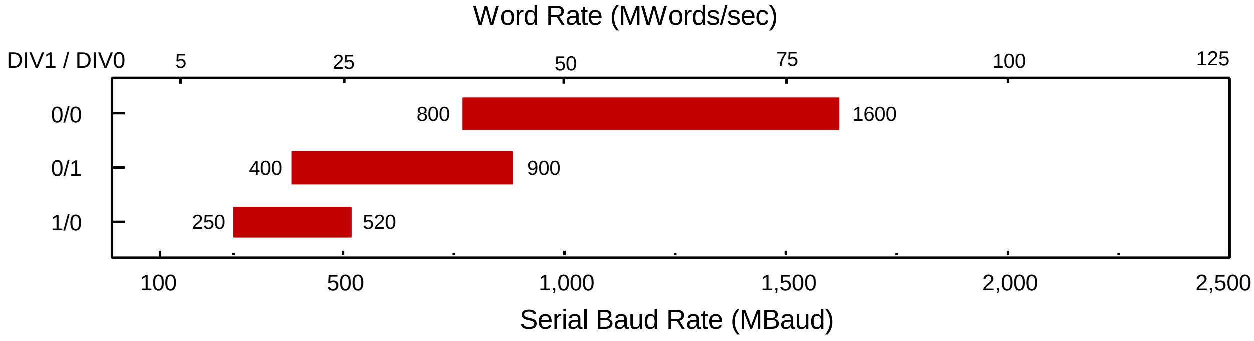


Figure 2. Typical Data Rates Showing Ranges of Operation[3]

Notes:
1. All values in this table are typical unless otherwise noted by (min) or (max). (min) indicates a minimum guaranteed value. (max) indicates a maximum guaranteed value.
2. All values in this table are expected for a BER less than 10^{-14}.
3. All values in this graph are typical values. As a result, two values (i.e. 250 and 1600) in the graph differ from the (min) and (max) values listed in the table above.

HDMP-1032 Tx Block Diagram

The HDMP-1032 transmitter was designed to accept 16 bit wide parallel words and transmit them over a high-speed serial line. The HDMP-1032 performs the following functions:

- Latching parallel word input
- Phase lock to TXCLK
- High speed clock multiplication
- Word encoding
- Parallel to Serial Multiplexing

PLL / Clock Generator

The Phase Lock Loop and Clock Generator are responsible for generating all the internal clocks needed by the transmitter to perform its functions. These clocks are based on a supplied word clock (TXCLK) and control signals (TXDIV1/0, TCLKENB). TXCLK is the incoming word clock. The PLL/Clock Generator locks on to this incoming rate and multiplies the word rate clock by 20 (16 word bits + 4 encoding bits). As lock is achieved, LOCKED is set high. The TXDIV1/0 pins configure the transmitter to accept incoming data words within the desired frequency range.

By setting TCLKENB high, the user may provide an external TTL serial clock at TXCLK. This clock replaces the internal VCO clock and is intended for diagnostic purposes only. This uncharacterized signal is used directly by the high-speed serial circuitry to output the serial data at speeds that are not within the VCO range.

C-Field and W-Field Encoder Logic

This logic determines what information is sent to the encoded word mux. If TXCNTL is high, the logic sends bits TX[0-13] and a C-Field (coding field) encoded as a control word regardless of the state of TXDATA. If TXCNTL is low and TXDATA is high, the logic sends TX[0-15] and a C-Field encoded as a data word. If neither TXCNTL nor TXDATA is set high, then the transmitter assumes the link is not being used. In this case, the logic submits an Idle Word to the encoded word mux to maintain the DC balance on the serial link and allow the receiver to maintain frequency and phase lock.

The C-Field logic, based on the inputs at TXCNTL, TXDATA, TXFLGENB and TXFLAG, supplies the four bits of the C-field to the encoded word mux. These bits contain information regarding the word type: Control, Data or Idle. In order for the TXFLAG bit to be used as an additional data bit, TXFLGENB must be set high on the Tx and RXFLGENB must be set high on the Rx. If scrambling of the encoding of the flag bit is desired, ESMPXENB pin must be set high on both the Tx and Rx. See Flag Descrambler section on next page for a more detailed description of the enhanced simplex mode.

The W-Field logic (word field) presents either bits TX[0-15] or an Idle Word to the encoded word mux.

Encoded Word Mux

The Word Mux accepts the four encoding bits from the C-Field and 16 data bits from the W-Field. These 20 bits of parallel information are then multiplexed to a serial line based on the internal high-speed serial clock.

Sign

The sign circuitry determines the disparity of the encoded word. Disparity is defined as the total number of high bits minus the total number of low bits.

Accumulator Block

This block is responsible for keeping track of total disparity of all previously sent words.

Invert Block

The Invert block is responsible for maintaining the DC balance of the serial line. It determines based on history and the sign of the current encoded word whether the current encoded word should be inverted to bring the serial line closer to the desired 50% duty cycle.

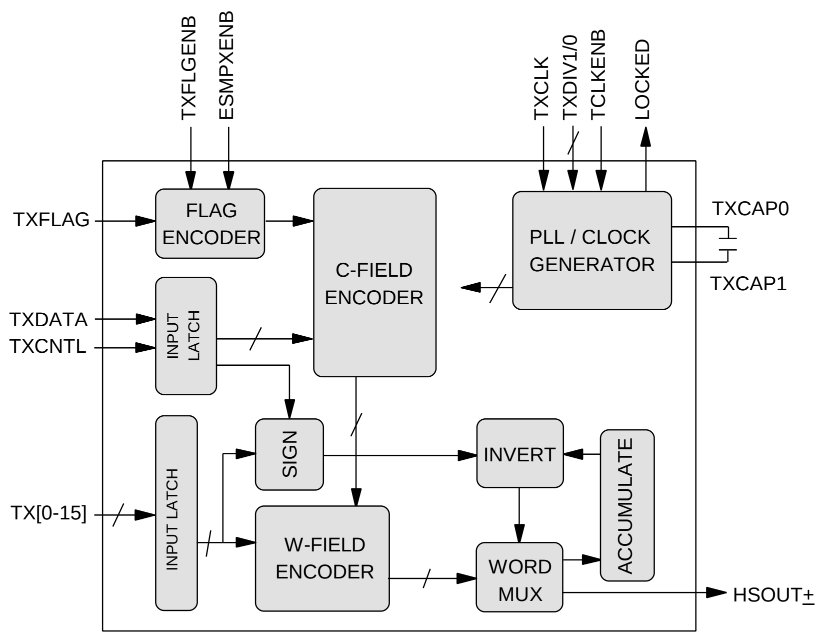


Figure 3. HDMP-1032 Transmitter Block Diagram

HDMP-1034 Rx Block Diagram

The HDMP-1034 receiver was designed to convert a serial data signal sent from the HDMP-1032 into either 16 or 17 bit wide parallel data. The HDMP-1034 performs the following functions:

- Frequency Lock
- Phase Lock
- Encoded Word Synchronization
- De-multiplexing
- Word Decoding
- Encoding Error Detection

Input Sampler and Clock-Data Recovery (CDR)

In order to compensate for any amplitude distortion present in the serial data signal, the high-speed inputs, HSIN+/-, are always equalized. The CDR block locks to the frequency of the REFCLK and to the phase of the sampled input signal. The recovered data is sent to the DEMUX block and a bit-rate clock is sent to the Clock Generator block. If the serial data signal is absent, the CDR block will maintain frequency lock onto REFCLK.

The RXDIV1/0 pins select the data rate range by dividing the VCO range by 1, 2 or 4. When RXDIV1/0 = 1/1, the internal VCO is bypassed and the test clock input TSTCLK can be used as the serial input.

Clock Generator

Using the recovered bit-rate clock, the CLOCK GENERATOR block generates all of the required internal clocks including the word rate clocks: RXCLK0/1.

Using the WORD ALIGN block's bit adjust output, the phase of the word-rate clocks is adjusted bit by bit for proper word alignment. For testing purposes this adjustment function can be disabled using the WSYNCDSB input; word alignment can also be forced using the #RESET pin.

Demultiplexer (DEMUX)

This block takes the recovered serial data from the CDR block and demultiplexes it into a 20-bit parallel word comprised of a 16-bit word-field and 4-bit code-field.

Decoder (DECODE)

This block decodes the 4-bit code-field and determines whether the 16-bit word-field is: normal or inverted; data, control, or idle words; or errors. The flag bit is also decoded from the data word.

Word Alignment (WORD ALIGN)

This block detects the error output of the decoder block. Upon detecting two consecutive errors, WORD ALIGN requests a bit adjustment to the clock generator (assuming WSYNCDSB=0).

If enhanced simplex mode is engaged (ESMPXENB=1), the Word Align block looks for a transition in the scrambled flag bit over a window of 32 words. If a transition is not detected, WORD ALIGN requests a bit adjustment to the clock generator (assuming WSYNCDSB=0).

When the bit adjustment output has been low for 64 up to 128 words, the RXREADY output goes high. If the bit adjustment output goes high, RXREADY immediately goes low.

Flag Descrambler (FLAG DESCRM)

This block descrambles the flag bit if the enhanced simplex mode is engaged (ESMPXENB=1); otherwise, the flag bit is unaltered. Scrambling ensures that the flag bit is dynamic and thus can be detected by the word alignment block. Scrambling of the flag bit provides an extra level of protection to guard against improper word alignment caused by static valid code-field bits being embedded within the data-field.

Enhanced simplex mode can be turned off (ESMPXENB=0) to make it compatible with previous versions of G-Link. With this mode turned off and TXFLGENB=1, the flag bit is sent unscrambled to the Rx. If TXFLGENB=0, the flag bit will alternate at the Tx. When RXFLGENB=0, the Rx will use this alternating flag for error checking.

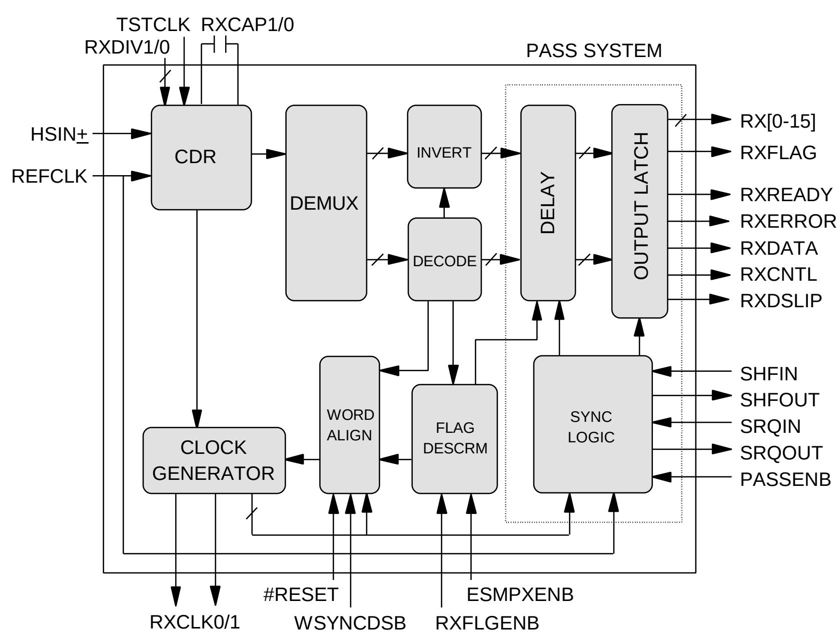


Figure 4. HDMP-1034 Receiver Block Diagram

Parallel Automatic Synchronization System (PASS)

As shown in Figure 4, this system consists of three blocks: the parallel delay block (DELAY), the output latch block (OUTPUT LATCH), and the synchronization logic block (SYNC LOGIC). This system was designed to provide a simple interface to the parallel outputs for a synchronous system.

Background

Traditionally, the parallel outputs are clocked out with the falling edge of RXCLK1 as shown in Figure 4.1. Since this clock is recovered from the serial data, this clock is synchronous with the remote clock at the Tx.

When the Tx and Rx clock are not synchronous, FIFO's are usually used to cross the frequency domains. The size of the FIFO and the frequency difference determine the maximum packet size of transmission.

When the clock from the Tx is synchronous with the Rx clock, data can be transmitted continuously without FIFO's since the parallel output data is synchronous with the local REFCLK. However, due to link distance and other physical variables, the relative phase of the REFCLK to the recovered data is unpredictable. Because of this unknown phase, the sampling of the recovered word must be adjusted so that the internal setup/hold times are not violated. Furthermore, in a multi-channel system, the setting of the phase must be consistent so that time slots across the channels are preserved.

The PASS system was designed to address these issues by sensing the phase difference between the local REFCLK with the recovered clock, and shifts the phase of the parallel output data with the DELAY block, such that it can be clocked out with the rising edge of the REFCLK. By adjusting the phase of the data word rather than REFCLK, the optimal setup time is achieved for the input latches of the chip interfacing to the Rx.

As the relative phase between the HSIN+/- input and the REFCLK drift slowly over time due to environmental variations, the PASS system is able to absorb this to some degree, and is able to reset and re-optimize the sampling when the margin is exceeded.

DELAY Block

The parallel DELAY block has an adjustable delay range of 20% to 80% of the data word. Its delay is controlled by the SYNC LOGIC block. This delay block is used for all of the data bits, flag bit, as well as the status bits.

OUTPUT LATCH Block

This block is a bank of positive edge triggered D-flip/flops. The clock is selected by the SYNC LOGIC block to be either the recovered clock RXCLK1 when the PASS system is disabled, or the REFCLK when the PASS system is enabled (PASSENB=1).

SYNC LOGIC Block

The SYNC LOGIC block's function is to compare the phase of the recovered data to REFCLK, to set the state of the DELAY block, to detect when the DELAY range has been exceeded, and to recover with a new DELAY setting. It is also designed to support a master/slave configuration in a multi-channel environment.

When RXREADY goes high, the optimal delay choice is determined at the shift output SHFOUT:

SHFOUT = 0	DELAY retract
SHFOUT = 1	DELAY extend

The actual setting of the DELAY block is determined with the shift input SHFIN.

When the phase of the REFCLK drifts to within 10% of the word boundary, the RXDSLIP output is set high, and a new choice of SHFOUT is chosen.

The shift request output SQROUT is set high when a RXDSLIP condition is detected, or if the shift request input SRQIN goes high.

Single Channel Configuration

In a single channel configuration, SHFIN is simply tied to SHFOUT as shown in Figure 4.2. The daisy chaining signal SRQIN is set low (grounded) and SRQOUT is left unconnected.

After RXREADY goes high, the DELAY block can absorb a phase variation between the serial input HSIN+/- and the REFCLK a minimum of ideally +/-4 serial bits, or 20% of the word period. This margin is reduced due to finite rise/fall times and setup times of the internal circuitry.

Multiple Channel Configuration

The connections for a multiple channel configuration are shown in Figure 4.3. The daisy-chain signals SRQIN and SRQOUT are used to allow each receiver's PASS system shift requests to propagate to the master, which is the last of the chain. The master then controls the shift command SHFOUT, which is tied common to the SHFIN of each receiver. The first SRQIN in the chain is grounded; the SRQOUT of the master as well as the SHFOUT outputs of the slave units are left unconnected.

When the internal parallel data boundary of the master, or any of the slaves come within 10% of the REFCLK, the RXDSLIP output is set high by the respective Rx, a shift request (SRQOUT=1) is issued which propagates to the master. The master again selects an optimum SHFOUT, which sets the DELAY blocks of all receivers consistently.

The phase absorption margin for a multiple channel configuration is the same as the single channel case, less the channel-to-channel skews.

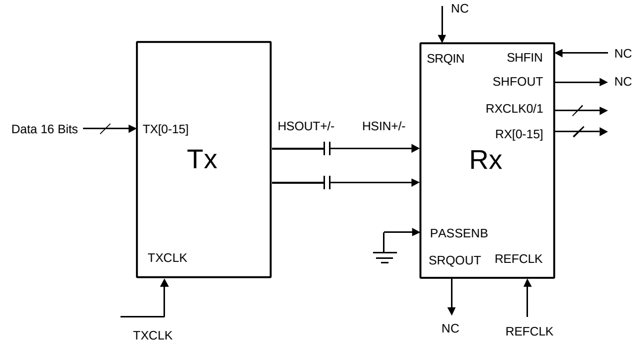


Figure 4.1. Traditional G-Link Configuration with PASS Disabled (PASSENB=0)
Recovered Data Words and RXCLK0/1 are Synchronous with TXCLK.

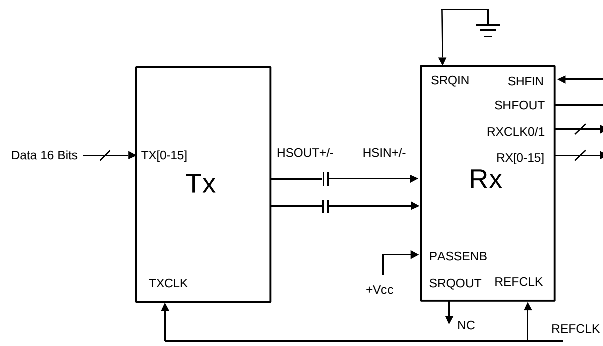


Figure 4.2. Single Channel Configuration with PASS Enabled (PASSENB=1)
Recovered Data Words and RXCLK0/1 are Synchronous with REFCLK.

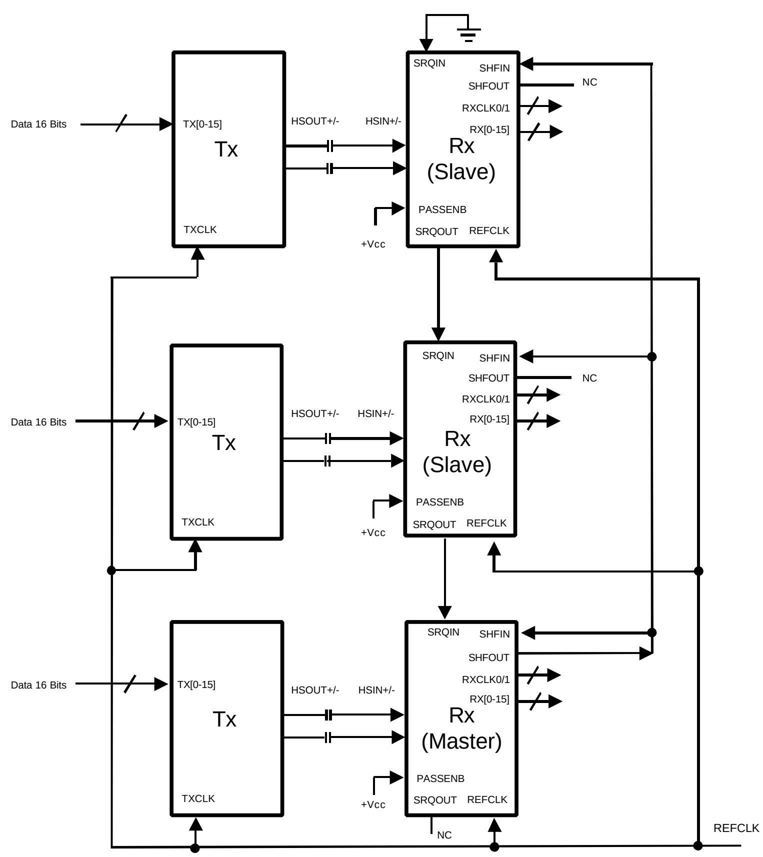


Figure 4.3. Multiple Channel Configuration with PASS Enabled (PASSENB=1)

HDMP-1032 (Tx) Timing

The Tx timing diagram is shown in Figure 5. Under normal operations, the Tx PLL locks an internally generated clock to the incoming TXCLK at which time LOCKED is set high. The incoming data, TX[0-15], TXDATA, TXCNTL, and TXFLAG are latched by this internal clock. The data must be valid for t_s before it is sampled and remain valid for a time t_h after it is sampled.

The setup and hold time parameters, t_s and t_h, are referenced to the rising edge of TXCLK.

The start of a word, bit TX[0], in the high speed serial output occurs after a delay of t_d after the rising edge of the TXCLK. The typical value of t_d is approximately one clock cycle.

HDMP-1032 (Tx) Timing Characteristics

Tc = 0 ^{o}C to +85 ^{o}C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_s	Setup Time, for TX[0-15], TXDATA , TXCNTL and TXFLAG Relative to Rising Edge of TXCLK.	nsec	2.5		
t_h	Hold Time, for TX[0-15], TXDATA , TXCNTL and TXFLAG Relative to Rising Edge of TXCLK.	nsec	2.5		

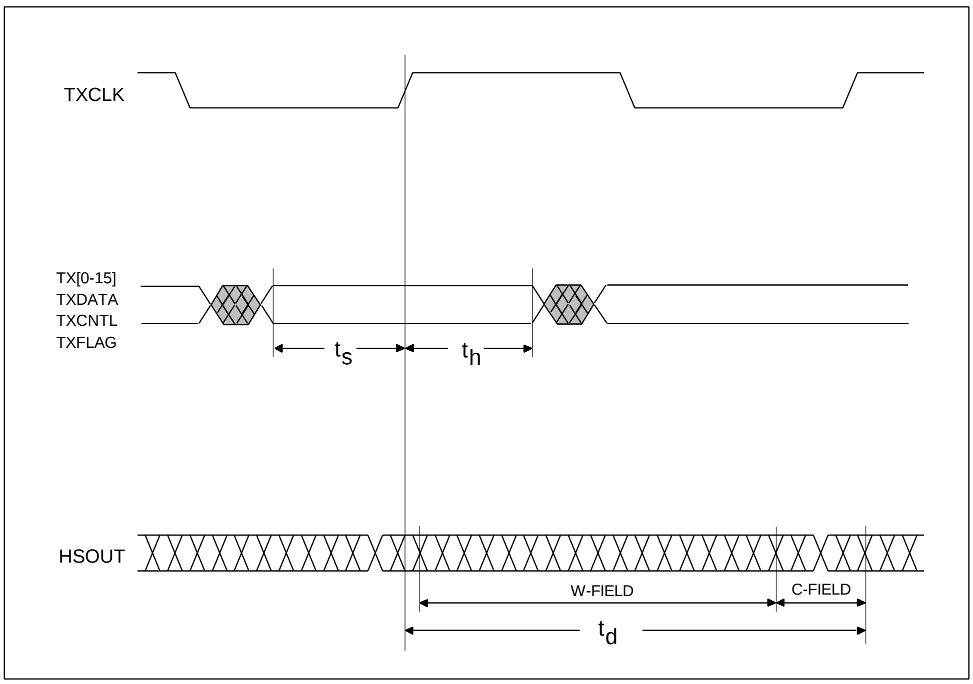


Figure 5. HDMP-1032 (Tx) Timing Diagram

HDMP-1034 (Rx) Timing

The Rx timing diagram when RXREADY=1 is shown in Figure 6. The serial data stream is deserialized into a parallel word at 1/20 the serial baud rate.

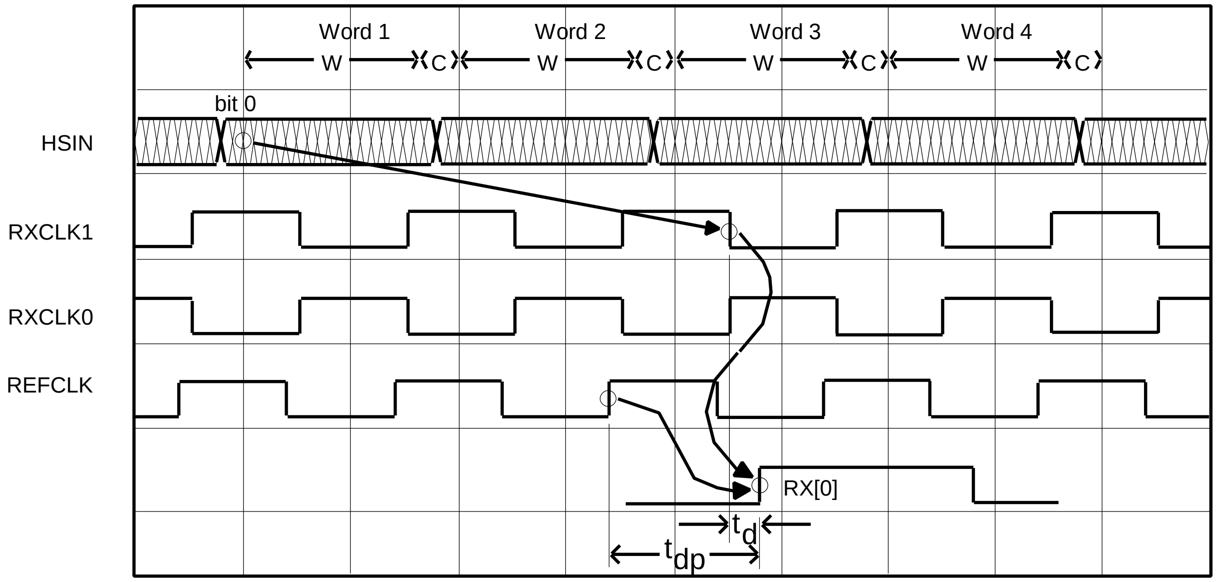
When the PASS system is disabled (PASSENB=0), there is a latency delay of two words from the input of the first serial bit of a word to the parallel outputs. The parallel outputs, RX[0-15], RXFLAG, RXREADY, RXERROR, RXDATA, RXCNTL and RXDSLIP are clocked out with the falling edge of RXCLK1 and appear after a delay of t_d. RXCLK1 and its complement RXCLK0 are both 50% duty cycle clocks.

When the PASS system is enabled (PASSENB=1), the timing of the parallel word is adjusted automatically +/- 30% of the word period so that it can be clocked out with the rising edge of REFCLK and appear after a delay of t_{dp}.

HDMP-1034 (Rx) Timing Characteristics

Tc = 0 ^{o}C to +85 ^{o}C, V_{CC} = 3.15V to 3.45V. Typical values are at Tc = 25 ^{o}C, V_{CC} = 3.3V

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_d	Synchronous Output Delay referenced to the falling edge of RXCLK1, PASS System Disabled (PASSENB=0).	nsec		2.0	3.5
t_{dp}	Synchronous Output Delay referenced to the rising edge of REFCLK, PASS System Enabled (PASSENB=1).	nsec		6.0	8.0
t_{sk}	Allowable skew between HSIN and REFCLK before PASS system resets, PASSENB=1.	nsec			20% word period – 0.4 nsec



Note: W = 16 Bit Word Field
C = 4 Bit Code Field

Figure 6. HDMP-1034 (Rx) Timing Diagram

HDMP-1032 (Tx), HDMP-1034 (Rx)
DC Electrical Specifications

Tc = 0 ^{o}C to +85 ^{o}C, V_{CC} = 3.15V to 3.45V, Typical values are at Tc = 25 ^{o}C, V_{CC} = 3.3V

Symbol	Parameter	Unit	Min.	Typ.	Max.
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed high signal for all inputs.	V	2.0		Vcc
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed low signal for all inputs.	V	0		0.8
$V_{OH,TTL}$	TTL Output High Voltage Level, I_{OH} = -400µA	V	2.2		Vcc
$V_{OL,TTL}$	TTL Output Low Voltage Level, I_{OL} = 500 µA	V	0		0.6
$I_{IH,TTL}$	Input High Current, V_{IN}=Vcc	µA			40
$I_{IL,TTL}$	Input Low Current, V_{IN}= 0 volts	µA			600
$V_{IP,H50}$	H50 Input Peak-To-Peak Differential Voltage	mV	200		
$V_{OP,BLL}$	BLL Output Peak-To-Peak Differential Voltage, Terminated with 50 Ω, ac coupled.	mV	1000		
$I_{CC,Tx}$	Transmitter V_{CC} Supply Current, 10 pF loading.	mA		180	
$I_{CC,Rx}$	Receiver V_{CC} Supply Current, 10 pF loading.	mA		200	

AC Electrical Specifications

Tc = 25 ^{o}C

Symbol	Parameter	Unit	Min.	Typ.	Max.
$t_{r,TTLin}$	Input TTL Rise Time, 0.8 to 2.0 volts	nsec		2	
$t_{f,TTLin}$	Input TTL Fall Time, 2.0 to 0.8 volts	nsec		2	
$t_{r,TTLout}$	Output TTL Rise Time, 0.8 to 2.0 volts, 10pF load	nsec			3.0
$t_{f,TTLout}$	Output TTL Fall Time, 2.0 to 0.8 volts, 10pF load	nsec			3.0
$t_{r, BLL}$	BLL Rise Time, Terminated with 50 Ω, ac coupled.[1]	psec		240	
$t_{f,BLL}$	BLL Fall Time, Terminated with 50 Ω, ac coupled.[1]	psec		240	
$VSWR_{i,H50}$	H50 Input VSWR			2:1	
$VSWR_{o,BLL}$	BLL Output VSWR			2:1	
T_{fa}	Transmitter & Receiver Frequency Acquisition Time at Power-on[2]	msec		4	
t_{Rx_wa}	Receiver Word Alignment Time	Words		300	

Latency

Tc = 25^{o}C

	Latency (Word Clock Cycles)		Latency Definition
	PASSENB = 0	PASSENB = 1	
Tx	1.4	1.4	Delay from the rising edge of TXCLK to the first bit TX[0] in the serial stream
Rx	2.6	3.0	Delay from the first bit RX[0] in the serial stream to the falling edge of RXCLK1 (or the rising edge of REFCLK if the PASS system is enabled, PASSENB=1)
Link	4.0	4.4	

Transmit Word Clock (TXCLK) and Receiver Reference Clock (REFCLK) Requirements

Tc = 0 ^{o}C to +85 ^{o}C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Unit	Min.	Typ.	Max.
F_{tol}	TXCLK and REFCLK Frequency Tolerance (REFCLK is referenced to TXCLK)	ppm	-100		+100
Symm	Symmetry (Duty Cycle)	%	40		60

Notes

1. Rise and fall times are measured between 20% and 80% of the voltage range.
2. Frequency acquisition time is independent of DIV1/DIV0 data rate range.

HDMP-1032 (Tx), HDMP-1034 (Rx)
Absolute Maximum Ratings

T_A = 25 ^oC except as specified. Operation in excess of any one of these conditions may result in permanent damage to the device.

Symbol	Parameter	Unit	Min.	Max.
V_{CC}	Supply Voltage	V	-0.5	5.0
$V_{IN,TTL}$	TTL Input Voltage	V	-0.7	5.5
$V_{IN,BLL}$	H50 Input Voltage	V	2.0	V_{CC}
$I_{O,TTL}$	TTL Output Source Current	mA		13
T_{stg}	Storage Temperature	^oC	-65	+150
T_J	Junction Temperature	^oC	0	+150
T_{max}	Maximum Assembly Temperature (10 seconds maximum)	^oC		+260

HDMP-1032 (Tx) Thermal Characteristics

T_A = 25 ^oC

Symbol	Parameter	Unit	Typ.
Θ_{jc}[1]	Thermal Resistance, Die to Case	$^oC/W$	8
P_D	Power Dissipation, V_{CC}= 3.3 V	mW	590

HDMP-1034 (Rx) Thermal Characteristics

T_A = 25 ^oC

Symbol	Parameter	Unit	Typ.
Θ_{jc}[1]	Thermal Resistance Die to Case	$^oC/W$	8
P_D	Power Dissipation, V_{CC} = 3.3 V	mW	660

I/O Type Definitions

I/O Type	Definition
I-TTL	Input TTL. Floats high when left open.
O-TTL	Output TTL
HS_OUT	50 Ω Matched Output Driver. Will drive AC coupled 50 Ω loads. All unused outputs should be AC coupled to a 50 Ω resistor to ground.
HS_IN	High Speed Input
C	Filter Capacitor Node
S	Power Supply or Ground

Note

1. Based on independent package testing by HP. Θ_{ja} for the HDMP-1032 and HDMP-1034 is 50 $^oC/W$. Θ_{ja} is measured on a standard 3"x3" two layer PCB in a still air environment. In order to determine the actual junction temperature in a given application, use the following formula: $T_J = T_C + (\Theta_{jc} \times P_D)$, where T_C is the case temperature measured on the top center of the package and P_D is the power being dissipated.

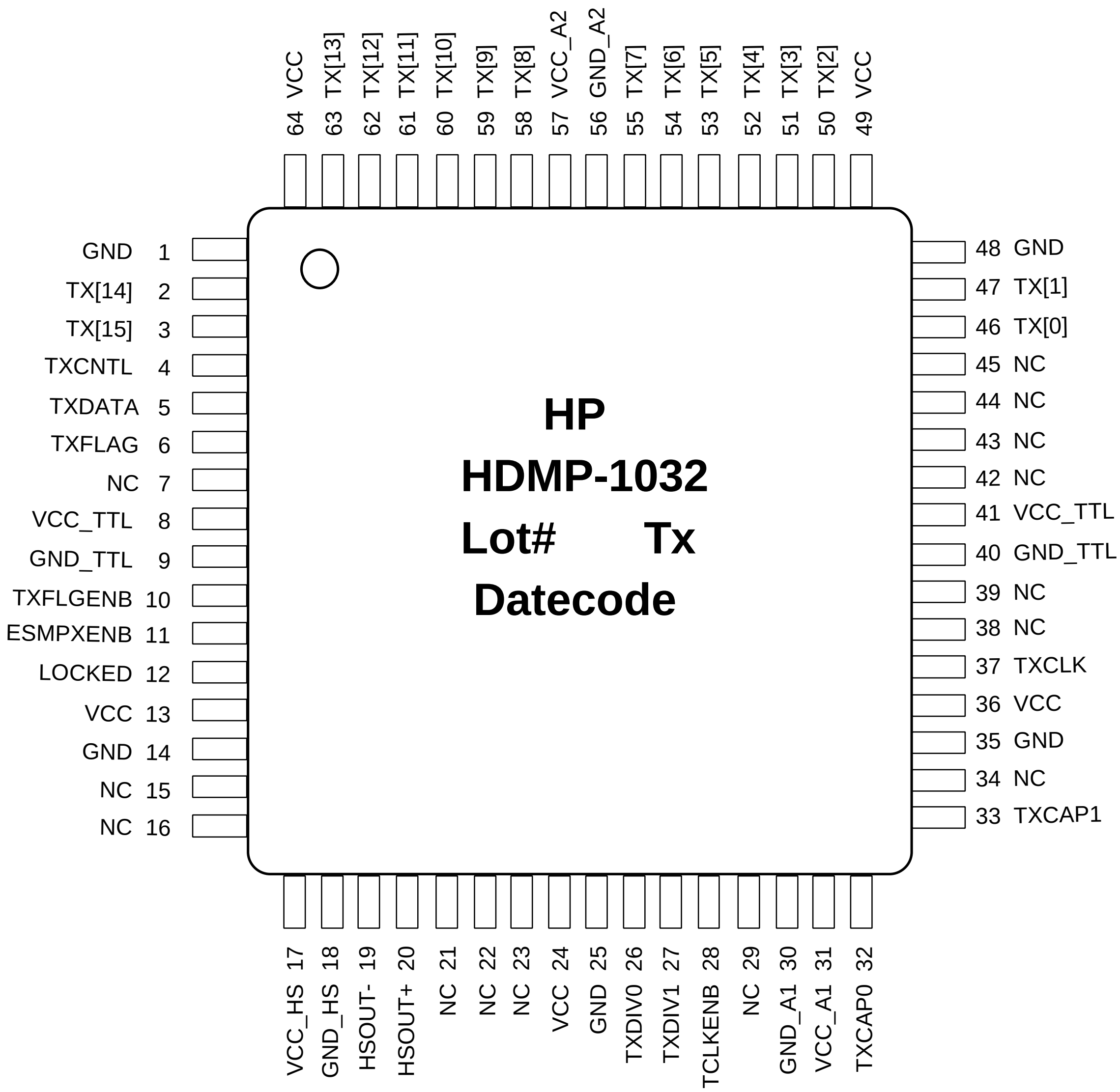


Figure 7. HDMP-1032 (Tx) Package Layout, Top View

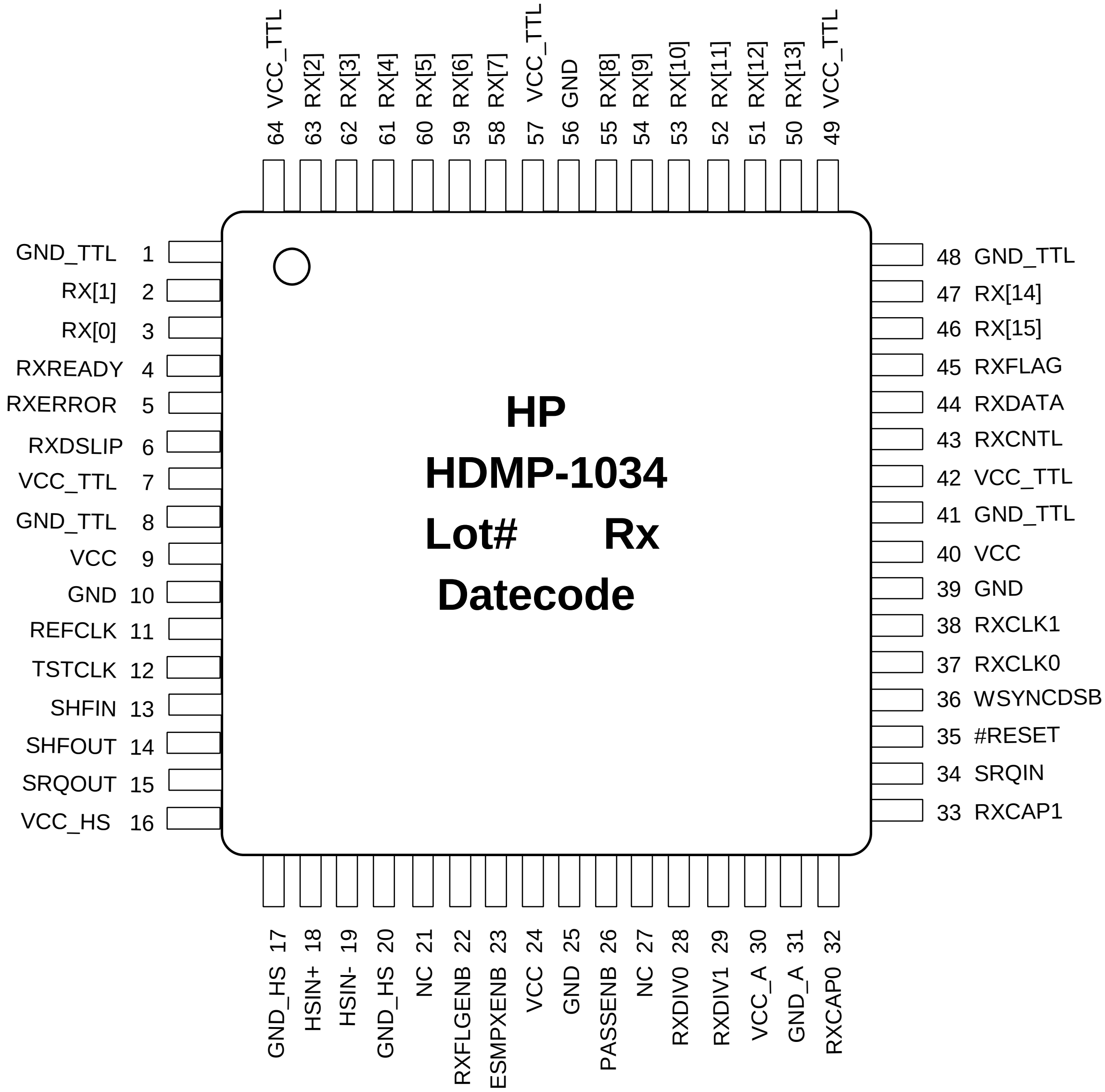


Figure 8. HDMP-1034 (Rx) Package Layout, Top View

HDMP-1032 (Tx) Pin Definition

USER MODE OPTIONS			
Name	**Pin**	**Type**	**Signal**
TXFLGENB	10	I-TTL	**Flag Bit Mode Select:** When this input is high**,** the TXFLAG bit input is sent as an extra 17th data bit during data word transfers. As an example, the flag bit can be used as an even or odd word indicator for 32 bit transmission. The RXFLGENB input on the Rx chip must be set to the same value as the TXFLGENB pin.
ESMPXENB	11	I-TTL	**Enhanced Simplex Mode Enable:** Enables scrambling of the Flag Bit encoding. The ESMPXENB pin on the Rx chip must be set to the same value. This mode should be enabled unless compatibility with previous versions of G-Link (i.e. HDMP-1024/1014) is desired which don't have this feature.
TXDATA	5	I-TTL	**Transmit Data Word:** This input tells the chip that the user has valid data to be transmitted. When this pin is asserted and TXCNTL is low, bits TX[0-15] and optionally TXFLAG are encoded and sent as a data word.
TXCNTL	4	I-TTL	**Transmit Control Word:** This input tells the Tx chip that the user is requesting a control word to be transmitted. When this pin is asserted, bits TX[0-13] are sent as a control word. If TXCNTL and TXDATA are asserted simultaneously, TXCNTL takes precedence. Idle words are transmitted if both TXDATA and TXCNTL are low.
HIGH SPEED SERIAL / PARALLEL I/O			
HSOUT+ HSOUT-	20 19	HS_OUT	**Serial Data Output:** These pins form a *buffer line logic* driver, which is a 50Ω terminated PECL compatible output.
TX[0] TX[1] TX[2] TX[3] TX[4] TX[5] TX[6] TX[7] TX[8] TX[9] TX[10] TX[11] TX[12] TX[13] TX[14] TX[15]	46 47 50 51 52 53 54 55 58 59 60 61 62 63 2 3	I-TTL	**Word Inputs:** When sending data words, TX[0-15] are serialized. When sending control words, TX[0-13] are serialized.
TXFLAG	6	I-TTL	**Flag Bit:** When TXFLGENB is active, this input is sent as an extra data bit in addition to the 16 data word bits. When TXFLGENB is not asserted, this input is ignored and an alternating internal flag bit is transmitted to allow the Rx chip to perform error detection during data word transfers. The Flag Bit is not sent when a control word is transmitted.

HDMP-1032 (Tx) Pin Definition (continued)

Name	Pin	Type	Signal
PLL / CLOCK GENERATOR			
TXCAP0 TXCAP1	32 33	C	**Loop Filter Capacitor:** A 0.1 uF min. loop filter capacitor, C2, must be connected across TXCAP0 and TXCAP1 for all combinations of TXDIV1/TXDIV0. See Figure 12.
TXCLK	37	I-TTL	**Transmit Word Clock Input:** When TCLKENB is low, this word rate clock input is phase locked and multiplied to generate the high-speed serial clock. When TCLKENB is high, the PLL is bypassed and TXCLK becomes the serial clock.
TXDIV0 TXDIV1	26 27	I-TTL	**VCO Divider Select:** These pins program the VCO divider chain to operate at full, half or quarter speed. See *Typical Operating Rates* table and Figure 2.
LOCKED	12	O-TTL	**Locked to TXCLK:** This pin goes high when the transmit PLL achieves frequency lock to the TXCLK signal.
POWER SUPPLY / GROUND			
VCC	13 24 36 49 64	S	**Logic Power Supply:** Normally 3.3 volts. This power supply is used for the internal transmitter logic.
VCC_TTL	8 41	S	**TTL Power Supply:** Normally 3.3 volts. Used for all TTL transmitter input and output buffer cells.
VCC_HS	17	S	**Serial Output Power Supply:** Normally 3.3 volts. Used for Serial Output pins.
VCC_A1 VCC_A2	31 57	S	**Analog Power Supply:** Normally 3.3 volts. Used for the analog section.
GND	1 14 25 35 48	S	**Ground:** Normally 0 volts. Tie to ground.
GND_TTL	9 40	S	**TTL Ground:** Normally 0 volts. Tie to ground.
GND_HS	18	S	**Serial Output Ground:** Normally 0 volts.
GND_A1 GND_A2	30 56	S	**Analog Ground:** Normally 0 volts.
TEST MODE / NO CONNECT PINS			
TCLKENB	28	I-TTL	**Enable External Serial Rate Clock Input:** When set high, this input causes the TXCLK input to be used for the serial transmit clock rather than the internal VCO clock. It is intended for diagnostic purposes and normally tied low.
NC	7 15 16 21 22 23 29 34 38 39 42 43 44 45		**No Connect:** These pins should be left unconnected.

HDMP-1034 (Rx) Pin Definition

Name	Pin	Type	Signal
USER MODE OPTIONS / STATUS			
RXFLGENB	22	I-TTL	**Flag Bit Mode Select:** When set high, the RXFLAG bit output is available to the user as an extra 17th data bit.
ESMPXENB	23	I-TTL	**Enhanced Simplex Mode Enable:** Enables descrambling of the Flag Bit encoding. The ESMPXENB pin on the Tx chip must be set to the same value. This mode should be enabled unless compatibility with previous versions of G-Link (i.e. HDMP-1022/1012) is desired which don't have this feature.
PASSENB	26	I-TTL	**Enable Parallel Automatic Synchronization System:** The parallel Rx data and control words are read out with REFCLK instead of the incoming word's parallel clock. The relative phase of the parallel output bits is internally adjusted so that they are clocked out with the rising edge of the REFCLK.
RXDATA	44	O-TTL	**Data Word Available Output:** This output indicates that the Rx chip word outputs RX[0-15] have a data word.
RXCNTL	43	O-TTL	**Control Word Available Output:** This output indicates that the Rx chip word outputs RX[0-13] have a control word.
HIGH SPEED SERIAL / PARALLEL I/O			
HSIN+ HSIN-	18 19	HS_IN	**Serial Data Input**
RX[0] RX[1] RX[2] RX[3] RX[4] RX[5] RX[6] RX[7] RX[8] RX[9] RX[10] RX[11] RX[12] RX[13] RX[14] RX[15]	3 2 63 62 61 60 59 58 55 54 53 52 51 50 47 46	O-TTL	**Word Outputs**
RXFLAG	45	O-TTL	**Flag Bit:** If both TXFLGENB and RXFLGENB have been asserted, this output indicates the value of the transmitted flag bit which can be used as an extra 17th data bit.
LINK STATUS			
RXREADY	4	O-TTL	**Receiver Ready:** This signal is asserted when the word alignment block has seen error-free code field nibbles for 64 up to 128 consecutive words. When ESMPXENB = 1, the toggling of the scrambled flag bit is also checked. RXREADY is de-asserted upon 2 consecutive errors in the code field or if the toggling of the flag bit is absent when ESMPXENB=1.
RXERROR	5	O-TTL	**Received Data Error:** Asserted when a word is received which does not correspond to either a *valid* Data, Control, or Idle Word encoding.

HDMP-1034 (Rx) Pin Definition (continued)

Name	Pin	Type	Signal
CDR / CLOCK GENERATOR			
RXCAP0 RXCAP1	32 33	C	**Loop Filter Capacitor:** A 0.1 uF min. loop filter capacitor, C2, must be connected across RXCAP0 and RXCAP1 for all combinations of RXDIV1/RXDIV0. See Figure 12.
REFCLK	11	I-TTL	**Reference Clock Input:** The Rx PLL uses this input for frequency lock. In addition, RX[0-15], RXFLAG, RXDATA, RXCNTL, RXREADY, RXERROR, and RXDSLIP are clocked out on the rising edge of REFCLK when PASSENB=1.
RXDIV0 RXDIV1	28 29	I-TTL	**VCO Divider Select:** These pins program the VCO divider chain to operate at full, half, or quarter speed. See *Typical Operating Rates* table and Figure 2.
RXCLK0 RXCLK1	37 38	O-TTL	**Recovered Word-Rate Clock Outputs:** These outputs are the PLL recovered word rate clocks. RX[0-15], RXFLAG, RXDATA, RXCNTL, RXREADY, RXERROR, and RXDSLIP are clocked out on the falling edge of RXCLK1 when PASSENB=0. RXCLK0 is the inverse of RXCLK1.
POWER SUPPLY / GROUND			
V_{CC}	9 24 40	S	**Power Supply:** Normally 3.3 volts. This power supply is used for all the core logic other than the output drivers.
VCC_TTL	7 42 49 57 64	S	**TTL Power Supply:** Normally 3.3 volts. Used for all TTL receiver input and output buffer cells.
V_{CC_HS}	16	S	**High Speed Supply:** Normally 3.3 volts. This supply is used to provide clean references for the high-speed inputs, HSIN+ and HSIN-.
VCC_A	30	S	**Analog Power Supply:** Normally 3.3 volts. This supply is used to feed power to the analog section of the chip.
GND	10 25 39 56	S	**Ground:** Normally 0 volts. Tie to ground.
GND_TTL	1 8 41 48	S	**TTL Ground:** Normally 0 volts. Tie to ground.
GND_HS	17 20	S	**High Speed Input Ground:** When tied to ground, the input impedance of HSIN+ and HSIN- are each matched to 50Ω. Additional 25Ω resistors can be added in series to ground to provide 75Ω input impedance. In order to obtain high impedance (high-Z) inputs for 1:N broadcast applications, 18KΩ series resistors to –5V are recommended.
GND_A	31	S	**Analog Ground:** Normally 0 volts. This ground is used for the analog PLL portion of the chip.

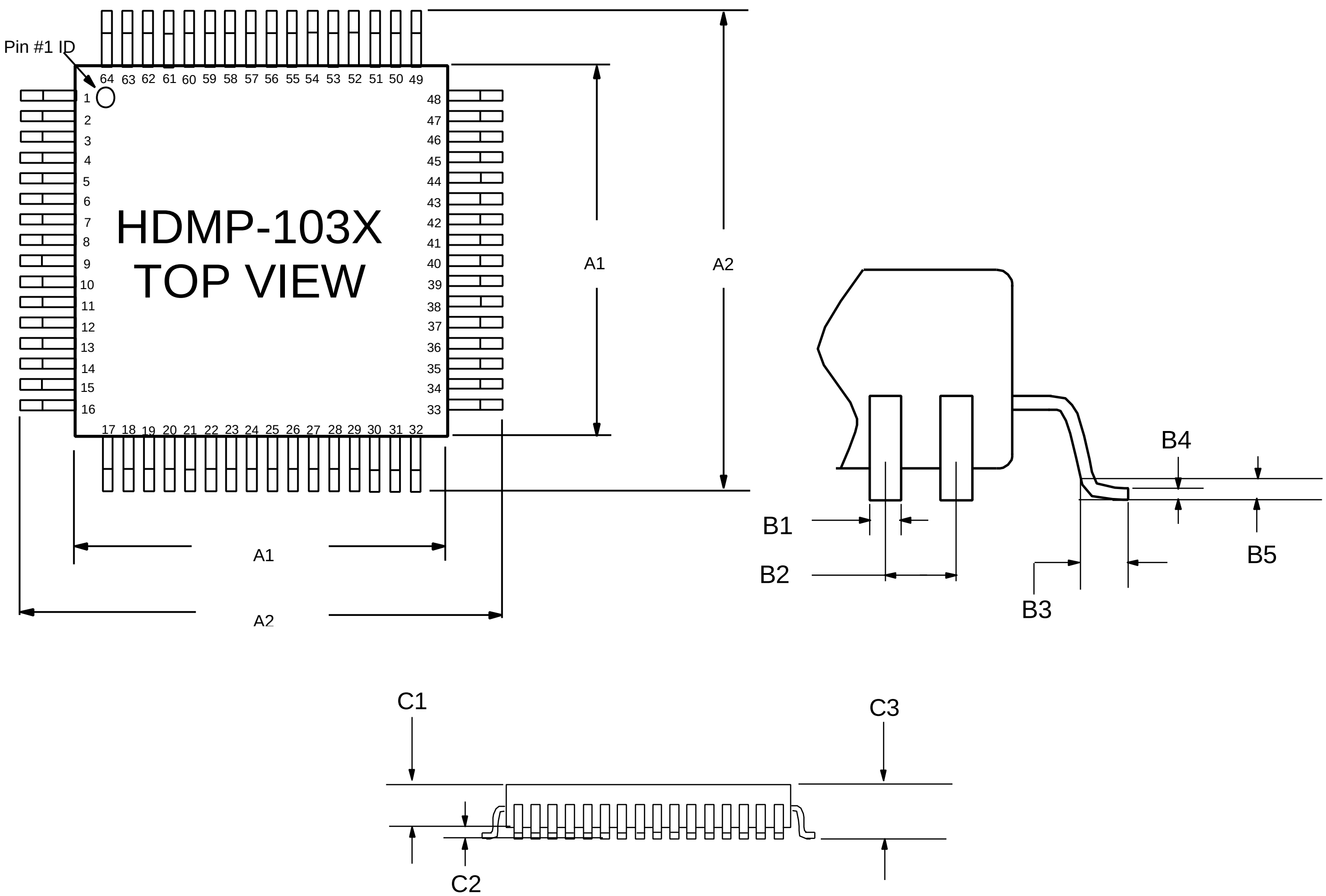
HDMP-1034 (Rx) Pin Definition (continued)

PASS SYSTEM			
Name	**Pin**	**Type**	**Signal**
RXDSLIP	6	O-TTL	**Rx Word Slip:** This output is asserted whenever the phase of the parallel word relative to the reference clock has exceeded the range of the internal delay, which results in a slippage of one word. See discussion of PASS system on page 7.
SHFIN	13	I-TTL	**Shift Input:** This input controls the delay of the parallel bits to be clocked out by REFCLK when PASSENB=1. In a single Rx configuration, SHFIN is connected to SHFOUT. In a multiple Rx configuration, all SHFIN are connected to the master's SHFOUT.
SHFOUT	14	O-TTL	**Shift Output:** This output, normally connected to SHFIN, is generated based on the relative phase between REFCLK and the internal parallel output bits.
SRQIN	34	I-TTL	**Shift Request Input:** In a daisy chain configuration, this input allows a shift request to be propagated to the master. SRQIN is connected to the SRQOUT of the previous Rx in a multi-receiver configuration.
SRQOUT	15	O-TTL	**Shift Request Output:** In a daisy chain configuration, this output is connected to the SRQIN input of the next receiver. SRQOUT goes high when a SRQIN=1 or when the relative phase between the REFCLK and the internal parallel bits requires a shift.
TEST MODE / NO CONNECT PINS			
TSTCLK	12	I-TTL	**External Serial Rate Clock Input:** When RXDIV1/0 = 1/1, this input is used in place of the normal VCO signal, effectively disabling the PLL and allowing the user to provide an external serial clock for testing. Pin is normally tied to VCC_TTL.
#RESET	35	I-TTL	**Reset:** When this active low input is asserted the word alignment is reset. Upon release (low to high) the normal word alignment process is reinstated. Pin used for test purposes and is normally tied to VCC_TTL.
WSYNCDSB	36	I-TTL	**Word Sync Disable:** When high, disables resynchronization to word edge upon errors encountered in the C-field of the incoming encoded word. Pin used for test purposes and is normally tied low.
NC	21 27		**No Connect:** These pins should be left unconnected.

Package Information

Item	Details
Package Material	Plastic
Lead Finish Material	85% Tin, 15% Lead
Lead Finish Thickness	300-800 µm
Lead Coplanarity	0.10 mm max

Mechanical Dimensions



All dimensions are in millimeters										
Part Number	A1	A2	B1	B2	B3	B4	B5	C1	C2	C3
HDMP-103X	14.00	17.20	0.35	0.80	0.88	0.17	0.25	2.00	0.25 MAX	2.35
TOLERANCE	±0.10	±0.25	±0.05	BASIC	+0.15/ -0.10	MAX		+0.10/ -0.05		MAX

Mechanical Dimensions of HDMP-1032/34

Appendix: Internal Architecture Information

Line Code Description

The HDMP-1032/1034 line code is Conditional Invert Master Transition (CIMT) as illustrated in Figure 9. The CIMT line code uses three types of words: Data words, Control words, and Idle words. Idle words are generated internally by the Tx when both TXDATA and TXCNTL are low. Each word consists of a Word Field (W-Field) followed by a Coding Field (C-Field). The C-Field has a master transition. Users can send arbitrary information carried by Data or Control Words. The DC balance of the line code is enforced automatically by the Tx. Idle words have a single rising edge at the master transition when operating in non-enhanced simplex mode.

The coding definitions are summarized in the table in page 22.

Note that the leftmost bit in each table is the first bit to be transmitted in time, while the rightmost bit is the last bit to be transmitted.

Data Word Codes

In Data Word mode, all 16 bits of the Tx are transmitted to the Rx, along with a flag bit. If TXFLGENB=1, then the user controls this bit with TXFLAG; otherwise it is internally set to alternate.

Control Word Codes

In Control Word mode, 14 bits are transmitted to the Rx. The lower 7 bits X0-X6 are sent in the w0-w6 space, and the upper 7 bits X7-X13 are sent in the w9-w15 space. Bits w7 and w8 are forced 01 for true, and 10 for inverted control words. The shifting of the word field is for backward compatibility with previous versions of G-Links chip sets.

Idle Word and Error Codes

Two Idle Words, IW1a and IW1b are provided. Unused word codes are mapped into Error States.

Enhanced Simplex Mode

In this mode (ESMPXENB=1), the flag bit is scrambled at the Tx and descrambled at the Rx. Since the Rx uses the scrambled flag bit for frame alignment, it is also defined for Control and Idle Words. However, the flag bit is only available to the user in the Data Word mode. The first bit w0 is also scrambled to aid word alignment.

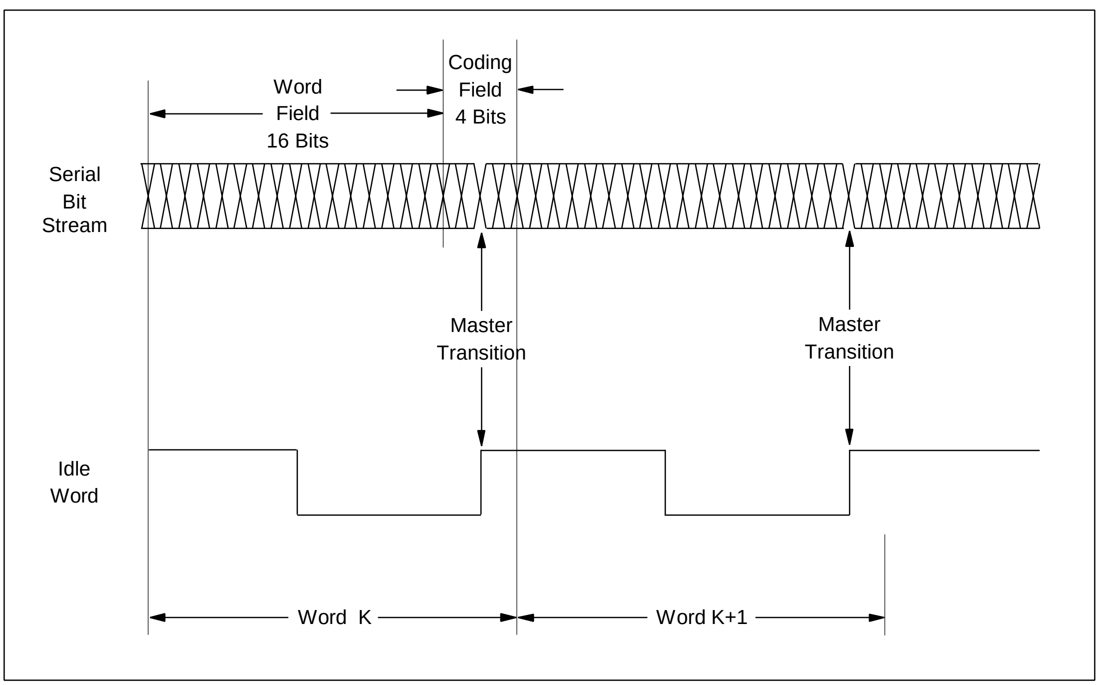


Figure 9. HDMP-1032/1034 (Tx/Rx Pair) Line Code

Coding[1] with ESMPXENB=0 (Compatible with previous G-Link chips, HDMP-1012/14, HDMP-1022/24)

Word Type	Flag	W-Field			C-Field
		w0 w1 w2 w3 w4 w5 w6	w7 w8	w9 w10 w11 w12 w13 w14 w15	c0 c1 c2 c3
Data Word Structure					
Data = True	0	X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15	1 1 0 1
Data = Inverted	0	#(X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15)	0 0 1 0
Data = True	1	X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15	1 0 1 1
Data = Inverted	1	#(X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15)	0 1 0 0
Control Word Structure					
Control = True		X0 X1 X2 X3 X4 X5 X6	0 1	X7 X8 X9 X10 X11 X12 X13	0 0 1 1
Control = Inverted		#(X0 X1 X2 X3 X4 X5 X6)	1 0	#(X7 X8 X9 X10 X11 X12 X13)	1 1 0 0
Idle Word Structure					
Idle Word 1a		1 1 1 1 1 1 1	1 1	0 0 0 0 0 0 0	0 0 1 1
Idle Word 1b		1 1 1 1 1 1 1	0 0	0 0 0 0 0 0 0	0 0 1 1
Detectable Error States					
		d d d d d d d	d d	d d d d d d d	d 0 0 d
		d d d d d d d	d d	d d d d d d d	d 1 1 d
		d d d d d d d	0 d	d d d d d d d	1 1 0 0
		d d d d d d d	1 1	d d d d d d d	1 1 0 0
		d d d d d d d	d d	d d d d d d d	1 0 1 0
		d d d d d d d	d d	d d d d d d d	0 1 0 1

Coding[1] with ESMPXENB=1

Word Type	Flag[2]	W-Field			C-Field
		w0[3] w1 w2 w3 w4 w5 w6	w7 w8	w9 w10 w11 w12 w13 w14 w15	c0 c1 c2 c3
Data Word Structure					
Data = True	0	X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15	1 1 0 1
Data = Inverted	0	#(X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15)	0 0 1 0
Data = True	1	X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15	1 0 1 1
Data = Inverted	1	#(X0 X1 X2 X3 X4 X5 X6	X7 X8	X9 X10 X11 X12 X13 X14 X15)	0 1 0 0
Control Word Structure					
Control = True	0	X0 X1 X2 X3 X4 X5 X6	0 1	X7 X8 X9 X10 X11 X12 X13	0 0 1 1
Control = Inverted	0	#(X0 X1 X2 X3 X4 X5 X6)	1 0	#(X7 X8 X9 X10 X11 X12 X13)	1 1 0 0
Control = True	1	X0 X1 X2 X3 X4 X5 X6	0 1	X7 X8 X9 X10 X11 X12 X13	0 1 0 1
Control = Inverted	1	#(X0 X1 X2 X3 X4 X5 X6)	1 0	#(X7 X8 X9 X10 X11 X12 X13)	1 0 1 0
Idle Word Structure					
Idle Word 1a	0	1 1 1 1 1 1 1	1 1	0 0 0 0 0 0 0	0 0 1 1
Idle Word 1b	0	1 1 1 1 1 1 1	0 0	0 0 0 0 0 0 0	0 0 1 1

Idle Word 1a	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1
Idle Word 1b	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1
Detectable Error States																					
		d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	0	0	d
		d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	1	1	d
		d	d	d	d	d	d	d	0	d	d	d	d	d	d	d	d	1	1	0	0
		d	d	d	d	d	d	d	1	1	d	d	d	d	d	d	d	1	1	0	0

Notes:
1. Xi denotes Txi or Rxi pin, # indicates Inversion, d denotes Don’t Care cases.
2. Flag bit is scrambled prior to sending. It is only available to the user in Data Word mode.
3. w0 is scrambled during transmission to further enhance word alignment.

Tx Operation Principles

The HDMP-1032 (Tx) is implemented monolithically in a high performance 25 GHz f_t silicon bipolar process. The Tx performs the following functions for link operation:

- Latching Parallel Word Input
- Phase Lock to TXCLK
- High-Speed Clock Multiplication
- Word Encoding
- Parallel to Serial Multiplexing

In normal operation, the Tx phase locks to a user supplied word rate clock and multiplies the frequency to produce the high-speed serial clock.

The Tx can accept either 16 or 17 bit wide parallel data and produce a 20 bit encoded word. Similarly, 14 bit control words can be transmitted in a 20 bit encoded word.

Tx Encoding

A simplified block diagram of the transmitter is shown in Figure 3. The PLL/Clock Generator locks onto the incoming word rate clock and multiplies it up to the serial clock rate. It also generates all the internal clock signals required by the Tx chip.

The data inputs, TX[0-15], as well as the control signals; TXDATA, TXCNTL and TXFLAG are latched in on the rising edge of an internally generated word rate clock. The word field is then encoded depending on the state of the TXDATA and TXCNTL signals. At the same time, the coding field is generated. At this point, the entire word has been constructed in parallel form and its sign is determined. This word sign is compared with the accumulated sign of previously transmitted bits to decide whether to invert the word. If the sign of the current word is the same as the sign of the previously transmitted bits, then the word is inverted. If the signs are opposite, the word is not inverted. No inversion is performed if the word is an idle word.

The Word Field and Coding Field are encoded depending on TXDATA, TXCNTL, TXFLAG, TXFLGENB as well as two internally generated signals, O/E and ACCMSB.

When TXFLGENB is high and ESMPXENB is low, O/E is equivalent to TXFLAG. This is equivalent to adding an additional bit to the data field. When TXFLGENB is also low, O/E alternates between high and low for data words. This allows the link to perform more extensive error detection when the extra bit is unused.

ACCMSB is the sign of the previously transmitted data. This is used to determine which type of Idle Word should be sent. When ACCMSB is low, IW1a is sent and when ACCMSB is high, IW1b is sent. This effectively drives the accumulated offset of transmitted bits back toward the balanced state.

Tx Phase-Lock Loop

The block diagram of the transmitter phase-lock loop (PLL) is shown in Figure 10. It consists of a sequential frequency detector, loop filter, VCO, clock generation circuitry and a lock indicator. The outputs of the frequency detector pass through a charge pump filter that controls the center frequency of the VCO. An external serial clock can be used instead of the VCO clock. This is accomplished by setting TCLKENB high and applying a serial rate clock to TXCLK. Note that this mode is used for diagnostic purposes only.

One of three frequency bands may be selected by applying the appropriate values to TXDIV1/0. The VCO or TXCLK frequency is divided by N where N is 1, 2, or 4 based on the settings of TXDIV1/0 as shown in the table below. This divided version of the VCO clock or TXCLK is used as the serial rate clock.

N	TXDIV1	TXDIV0
1	0	0
2	0	1
4	1	X

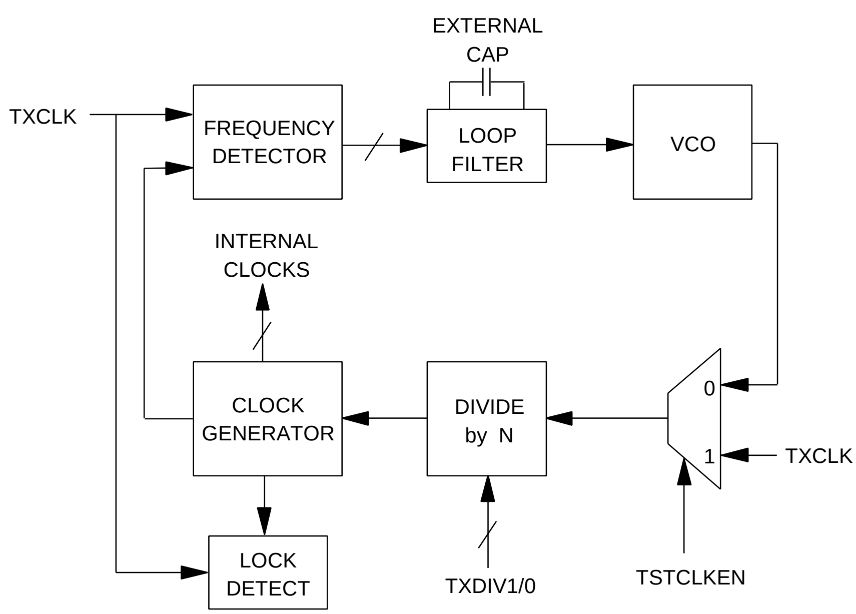


Figure 10. HDMP-1032 (Tx) Phase-Lock Loop

Rx Operation Principles

The HDMP-1034 (Rx) is implemented monolithically in a high performance 25 GHz f_t silicon bipolar process. The Rx accepts a serial stream of 20 bit Conditional Invert with Master Transition (CIMT) line code words and outputs parallel 16 bit / 17 bit Data Words or 14 bit Control Words. The Rx performs the following functions for link operation:

- Frequency Lock
- Phase Lock
- Word Synchronization
- Demultiplexing
- Word Decoding
- Error Detection
- Automatic Parallel Word Phase Adjustment

Rx Data Path

Figure 4 shows a simplified block diagram of the receiver. The data path consists of an Input Sampler, a Word Demultiplexer, a Coding Field (C-Field) Decoder, and a Word Field (W-Field) Decoder. An on-chip phase-lock loop (PLL) is used to extract timing reference from the serial input (HSIN+/-). The PLL includes a Phase-Frequency Detector, a Loop Filter, and a voltage controlled oscillator (VCO). All the Rx internal clock signals are generated from a Clock Generator that is driven by either the internal VCO or an external signal, TSTCLK, depending on whether both RXDIV1/0 are set high.

Rx Phase-Lock Loop

A detailed block diagram for the Rx Phase Lock Loop is shown in Figure 11. A frequency detector locks the VCO to the reference clock. Once this is achieved, a lock indication engages the phase detector, which maintains phase lock of the high speed incoming bits to that of the internal bit clock.

The integrator, which requires one external capacitor, controls the frequency of the VCO. The output of the VCO is fed into a Range Selector block, which further divides the VCO clock to the bit rate clock. The RXDIV1/0 inputs select between divide by 1, 2, or 4 ranges, as well as a test clock bypass mode. The bit rate clock then drives the clock generator, which provides clocks to the entire chip.

Rx Decoding

In Figure 4, the word demultiplexer de-serializes the recovered serial data from the Input Sampler, and outputs the resulting parallel data one word at a time. Every word is composed of a 16-bit Word Field (W-Field) and a 4-bit Coding Field (C-Field). The C-Field (c0-c3) together with the two center bits of the W-Field (w7 and w8) are then decoded by the C-Field decoder to determine the content of the word. The W-Field decoder is controlled by the outputs of the C-Field decoder. If an inverted Data Word or Control Word is detected, the W-Field decoder will automatically invert the W-Field data. If a Control Word is detected, the W-Field decoder will shift the bottom half of the W-Field so that the outputs are at pins RX[0-13]. RXDATA = 1 indicates that data word is detected by the receiver. RXCNTL = 1 indicates that a control word is detected by the receiver. An idle word is detected by the receiver if RXDATA = 0, RXCNTL = 0, and RXERROR = 0.

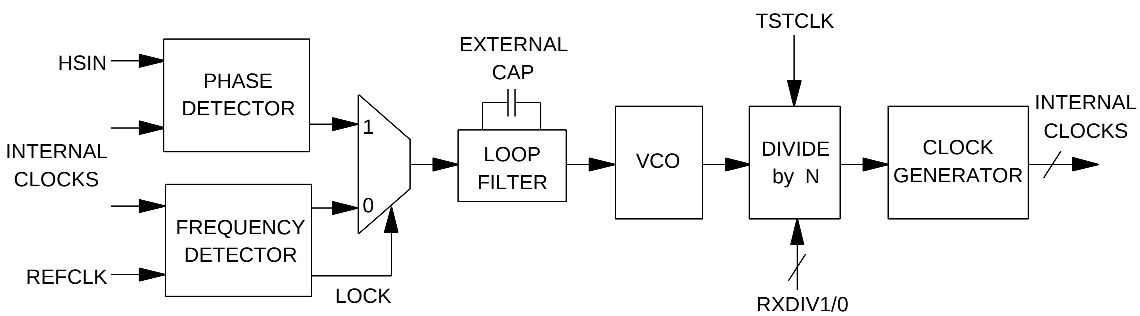


Figure 11. HDMP-1034 (Rx) Phase-Lock Loop

Integrator Capacitor and Supply Bypassing / Grounding

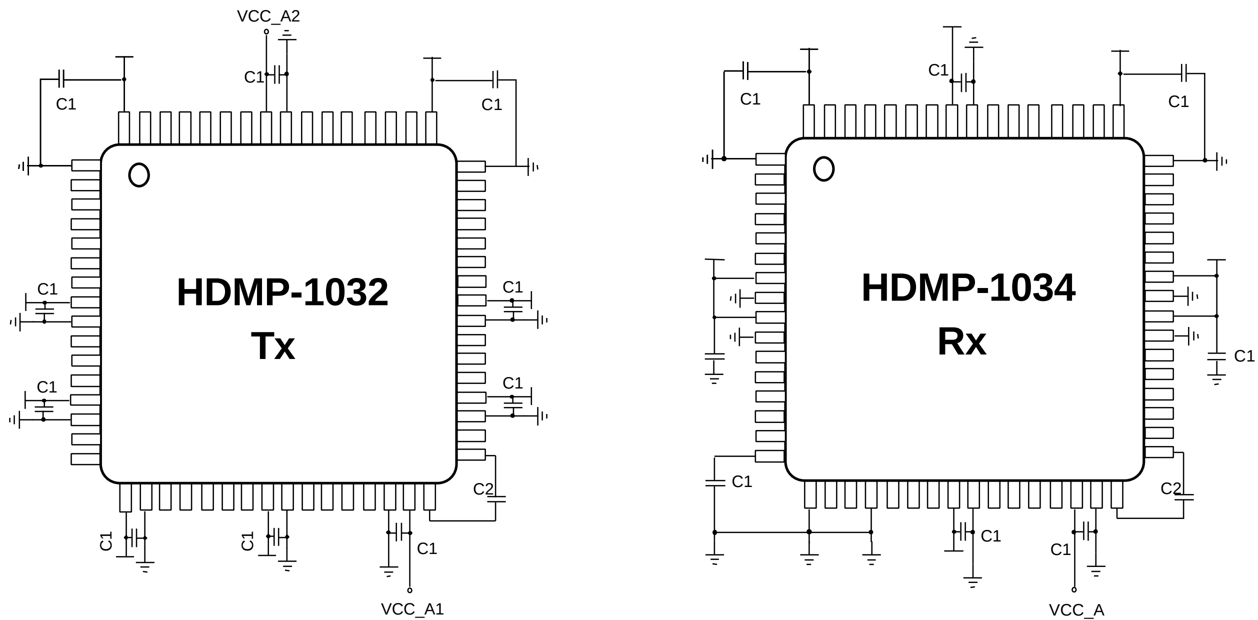
Figure 12 shows the PLL integrator capacitors, power supply capacitors and required grounding for the Tx and Rx chips.

Integrator Capacitor

An integrator capacitor (C2) is required by both the Tx and Rx for them to function properly. This cap is used by the PLL for frequency and phase lock, and directly sets the stability and lockup times. A 0.1 uF capacitor is recommended for each DIV1/0 setting.

Supply Bypassing / Grounding

The HDMP-1032/34 chipset has been tested to work well with a single power plane, assuming that it is a fairly clean power plane. As a result, all of the separate power supplies (VCC, VCC_TTL, and VCC_HS) can be connected onto this plane. The bypassing of VCC to ground should be done with a 0.1 μF capacitor (C1).



Note: VCC_A pins supply voltage should come from a low noise source.
C1 = Bypass Capacitor 0.1 uF
C2 = PLL Integrator Capacitor 0.1 uF

Figure 12. HDMP-1032 (Tx) and HDMP-1034 (Rx) Power Supply Pins

TTL and High Speed I/O

I-TTL and O-TTL

These I/O pins are TTL compatible. A simplified schematic diagram of the I/O cells is shown in Figure 13.

High-Speed Interface:
HS_IN and HS_OUT

The simplified schematic diagrams of HS_IN and HS_OUT are shown in Figure 14. The HS_IN input cell is implemented with internal 50Ω resistors between the differential input lines HSIN+/- to GND_HS.

The GND_HS pins are normally tied to ground to provide 50Ω input impedance. Additional 25Ω series resistors can be added to increase the impedance to 75Ω. For 1:N broadcast applications, 18KΩ series resistors can be inserted between GND_HS and –5V to provide an effective high impedance.

The HSIN+/- inputs have internal bias provided and the signals are AC coupled in with 0.1uF capacitors. It is recommended that differential signals be applied across the HSIN+/- inputs (Figure 15a), although a single-ended connection is also acceptable. In this case, the unused input must be terminated with 50Ω AC coupled to ground.

The HS_OUT output cell is designed to deliver PECL swings directly into 50Ω. The output impedance is matched to 50Ω and has a VSWR of less than 2:1 to above 2 GHz. This output is ideal for driving the HS_IN input through a 50Ω cable and a 0.1 uF coupling capacitor. The HS_OUT driver can also be connected directly into a high-speed 50Ω oscilloscope. For optimum performance, both outputs should see the same impedance. It is necessary that all HS_OUT outputs be terminated into 50Ω. Figure 15 shows various methods of interfacing HS_OUT to HS_IN and standard PECL logic.

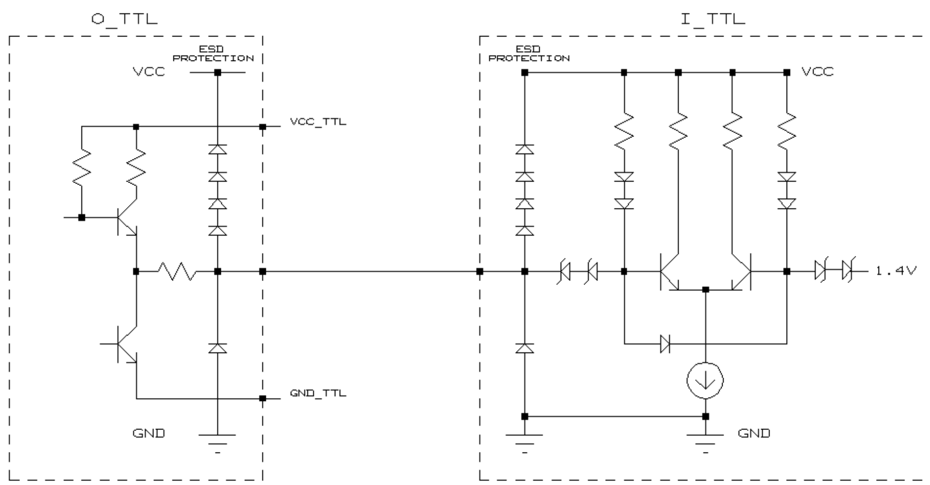


Figure 13. O-TTL and I-TTL Simplified Circuit Schematic

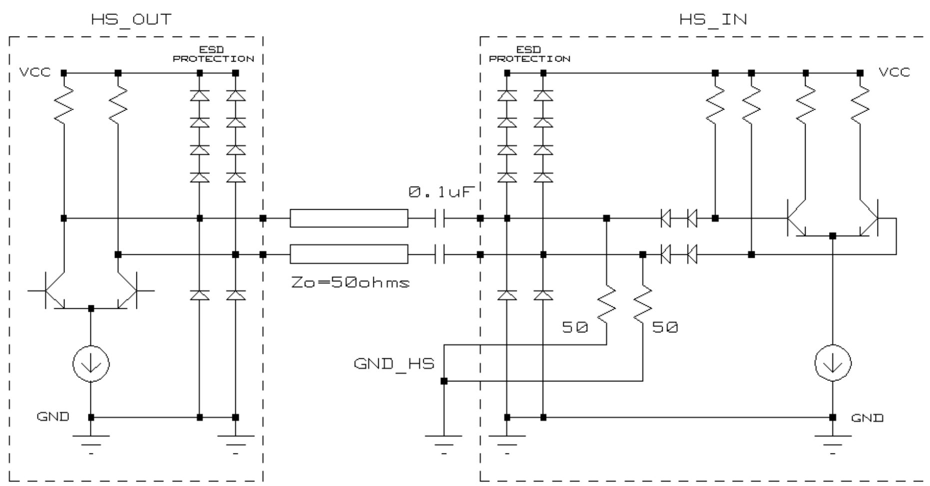
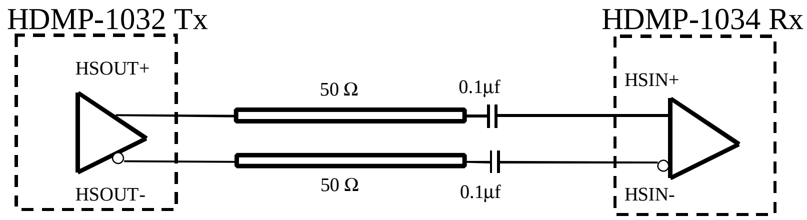
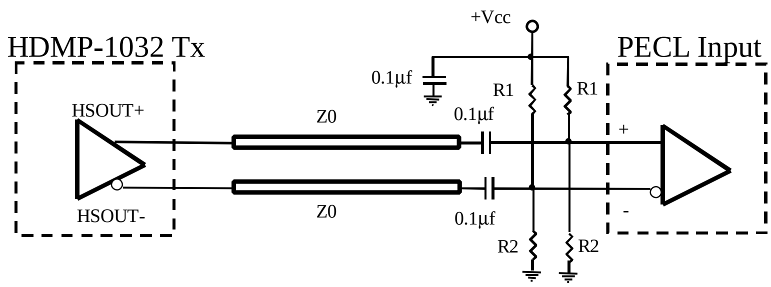


Figure 14. HS_OUT and HS_IN Simplified Circuit Schematic



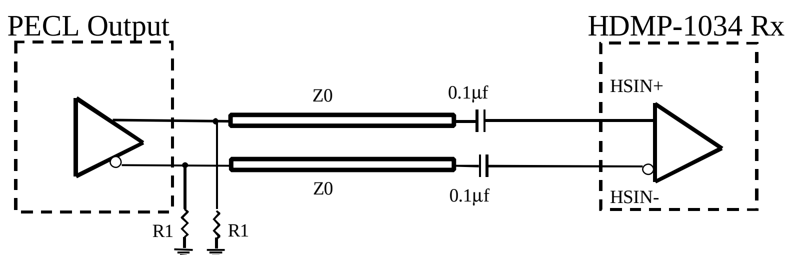
a) G-Link Tx to Rx Interconnection

Note that no external terminations or bias resistors are required.



b) Differential Drive to Generic PECL Input

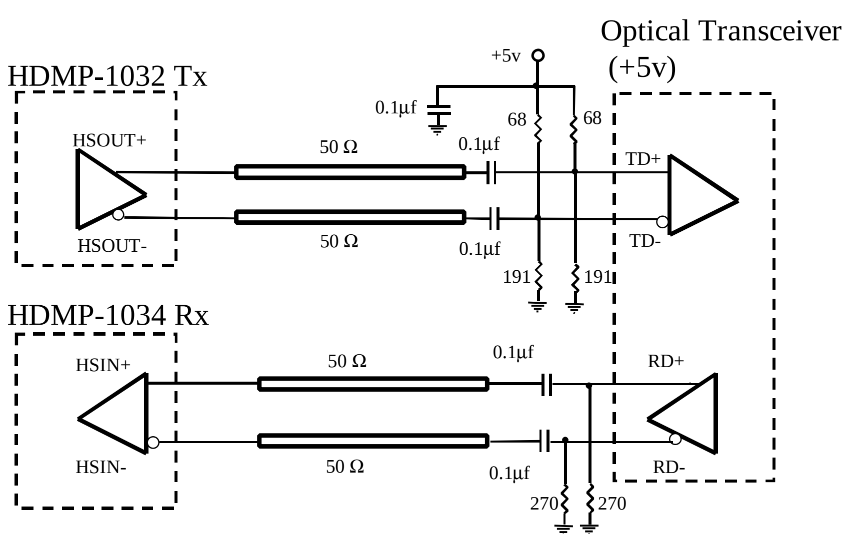
The Thevenin equivalent resistance is equal to the transmission line impedance (Z0) and provides proper DC Bias to the PECL inputs.



c) Generic PECL Output to G-LINK Rx Input

Resistor value R1 sets proper bias for the PECL output stage.

The G-Link Rx is internally terminated and doesn't require external bias or termination resistors.



d) G-Link Interface to Optical Transceiver

Figure 15. Methods of Interfacing HS_OUT and HS_IN

Nomenclature Changes between HDMP-1032/34 and HDMP-1022/24

In previous versions of G-Link such as the HDMP-1022/24 each parallel unit of data was called a **frame**. This has been changed to a **word** with the HDMP-1032/34. Frame usually stands for a series of words that form a logical unit. For example, each unit of PPP unit is called a frame. It consists of a header and a checksum at the end.

The encoded 20 bit entity for the HDMP-1022/24 was composed of a data field and also a control field. This was confusing because the data field contained data frames and control frames. In other words control and data were used in two different contexts which left the reader to identify which of the two meanings was meant. The encoded word was split into a word field and an encoding field.

With the HDMP-1032/34 we have:

- control words
- data words
- word field
  - where one may find control words or data words
- encoding field

In addition with the HDMP-1032/34, fill frames have been changed to idle words following the custom used in Fibre Channel and Gigabit Ethernet where idles are inserted if no information is being fed to the transmitter.

Pin names have been changed to specify if they belong to the transmitter (Tx) or the receiver (Rx). In addition, some names have been changed to names analogous to those used in Fibre Channel and Gigabit Ethernet. Examples are TXCLK instead of STRBIN and RXCLK instead of STRBOUT. A pin cross reference table for the HDMP-1032/34 & HDMP-1022/24 is provided in the table on the next page.

Pin Cross Reference Table

HDMP-1032 (Tx)		HDMP-1022 (Rx)
Pin	Name	Name
1	GND	
2	TX[14]	D14
3	TX[15]	D15
4	TXCNTL	CAV*
5	TXDATA	DAV*
6	TXFLAG	FLAG
7	NC	
8	VCC_TTL	
9	GND_TTL	
10	TXFLGENB	FLAGSEL
11	ESMPXENB	
12	LOCKED	
13	VCC	
14	GND	
15	NC	
16	NC	
17	VCC_HS	
18	GND_HS	
19	HSOUT-	DOUT*
20	HSOUT+	DOUT
21	NC	
22	NC	
23	NC	
24	VCC	
25	GND	
26	TXDIV0	DIV0
27	TXDIV1	DIV1
28	TCLKENB	EHCLKSEL
29	NC	MDFSEL
30	GND_A1	
31	VCC_A1	
32	TXCAP0	CAP0B
33	TXCAP1	CAP1B
34	NC	
35	GND	
36	VCC	
37	TXCLK	STRBIN
38	NC	
39	NC	
40	GND_TTL	
41	VCC_TTL	
42	NC	
43	NC	
44	NC	
45	NC	
46	TX[0]	D0
47	TX[1]	D1
48	GND	
49	VCC	
50	TX[2]	D2
51	TX[3]	D3
52	TX[4]	D4
53	TX[5]	D5
54	TX[6]	D6
55	TX[7]	D7
56	GND_A2	
57	VCC_A2	
58	TX[8]	D8
59	TX[9]	D9
60	TX[10]	D10
61	TX[11]	D11
62	TX[12]	D12
63	TX[13]	D13
64	VCC	

HDMP-1034 (Rx)		HDMP-1024 (Rx)
Pin	Name	Name
1	GND_TTL	
2	RX[1]	D1
3	RX[0]	D0
4	RXREADY	LINKRDY*
5	RXERROR	ERROR
6	RXDSLIP	
7	VCC_TTL	
8	GND_TTL	
9	VCC	
10	GND	
11	REFCLK	
12	TSTCLK	TCLK
13	SHFIN	
14	SHFOUT	
15	SRQOUT	
16	VCC_HS	
17	GND_HS	
18	HSIN+	DIN
19	HSIN-	DIN*
20	GND_HS	
21	NC	
22	RXFLGENB	FLAGSEL
23	ESMPXENB	
24	VCC	
25	GND	
26	PASSENB	
27	NC	TCLKSEL
28	RXDIV0	DIV0
29	RXDIV1	DIV1
30	VCC_A	
31	GND_A	
32	RXCAP0	CAP0B
33	RXCAP1	CAP1B
34	SRQIN	
35	#RESET	
36	WSYNCDSB	
37	RXCLK0	STRBOUT
38	RXCLK1	
39	GND	
40	VCC	
41	GND_TTL	
42	VCC_TTL	
43	RXCNTL	CAV*
44	RXDATA	DAV*
45	RXFLAG	FLAG
46	RX[15]	D15
47	RX[14]	D14
48	GND_TTL	
49	VCC_TTL	
50	RX[13]	D13
51	RX[12]	D12
52	RX[11]	D11
53	RX[10]	D10
54	RX[9]	D9
55	RX[8]	D8
56	GND	
57	VCC_TTL	
58	RX[7]	D7
59	RX[6]	D6
60	RX[5]	D5
61	RX[4]	D4
62	RX[3]	D3
63	RX[2]	D2
64	VCC_TTL	